Integrated SiC Anode Switched Thyristor Modules for Smart-Grid Applications

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Abstract: Silicon Carbide Anode Switched Thyristors (ASTs) overcome major limitations of conventional Si and SiC IGBT and GTO Thyristor solutions by providing robust, latch-up free turn-off at high currents, current saturation in the output characteristics, and a wide safe operating area (SOA) through series current controlled device turn-off. In this work, detailed static and switching characteristics of 6.5 kV-class SiC ASTs are reported, which include a low on-state voltage drop of 4 V at 100 A/cm^2, slight positive temperature co-efficient of Von, current saturation at > 100 A Cathode currents and fast turn-on and turn-off times of 500 ns while switching 1300 V and 20 A.

Introduction

The SiC Anode Switched Thyristor (AST) is developed by GeneSiC for high efficiency power conversion at > 13 kV, > 50 A and > 10 kHz ratings for applications including Flexible AC transmission systems (FACTS), Fault-Current Limiters, AC-DC converters, and Static VAR Compensators. In an AST, the turn-on and turn-off of a high-voltage SiC GTO Thyristor is accomplished by high-current Si MOSFETs controlled by commercially available gate drivers. In contrast to conventional SiC Thyristors, the SiC AST offers MOS gate control, a wider safe operating area (SOA) due to latch-up free high-current turn-off, current saturation capability and fast switching speeds. The AST eliminates the need for turn-on and turn-off snubber circuitry, which is essential for convenient operation of conventional Thyristors. The detailed on-state, blocking voltage and switching characteristics of 6.5 kV-rated SiC ASTs are presented in this paper.

Design and Fabrication of the SiC AST

A schematic of the AST circuit is shown in Figure 1(a) and a photograph of the fabricated AST module is shown in Figure 1(b). The AST is turned-on from its blocking state by providing a negative Gate current trigger pulse, which latches-on the SiC Thyristor and turns-on a p-MOSFET connected in series with the Thyristor Anode. To turn-off the AST, the Gate pulse is withdrawn, which turns off the p-MOSFET and subsequently turns on a diode-connected n-MOSFET connected in series with the Thyristor Gate electrode, when the threshold voltage of the n-MOSFET is exceeded. The turning-off of the p-MOSFET and turning-on of the n-MOSFET commutates the entire Anode current to the Gate path of the AST. This results in a collapse of the "Thyristor Action", and the AST turns-off like an open base npn transistor with a rapid, unity-gain turn-off.

The key design parameters for the SiC AST include the selection of appropriate Si N-Channel and P-Channel MOSFETs with the appropriate voltage/current ratings and suitable threshold voltages, such that they turn-on and turn-off at appropriate times during the AST switching and do not introduce excessive series resistance during on-state operation. In the present work, a 4.1 mm x 4.1 mm SiC Thyristor with active area of 7.3 mm^2, 75 V/90 A Si n-MOSFETs with a Gate threshold voltage of ≈ +4 V and a 85 V/96 A Si p-MOSFETs were used in the AST circuit. A key feature of this work was the co-packaging of the Si MOSFETs and the SiC Thyristor on the same baseplate with the appropriate voltage isolation necessary for high blocking voltages, as shown in Figure 1 (b).

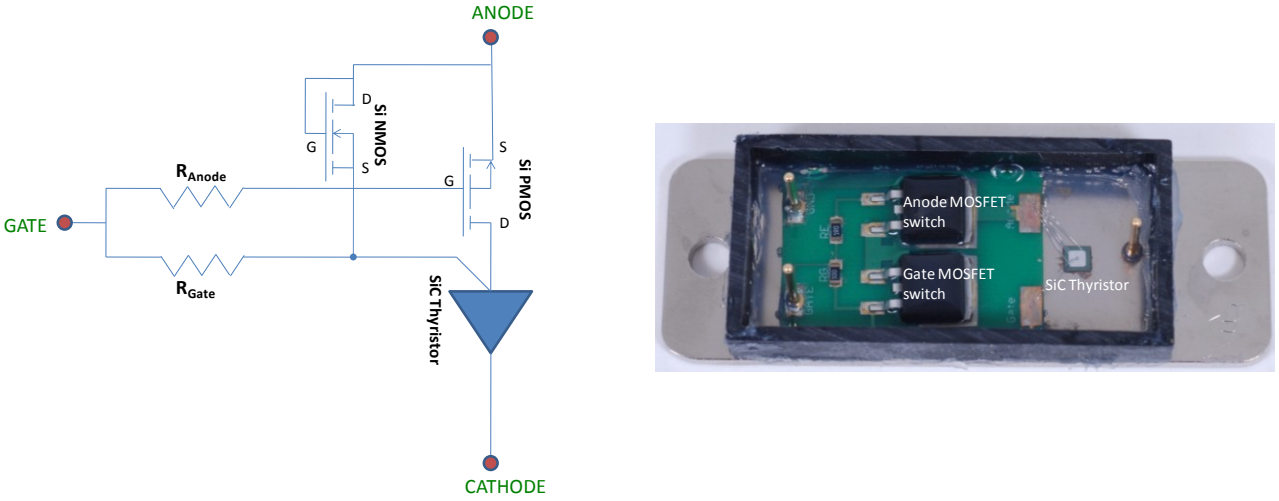

Figure 1 (Left, a) Simplified Circuit-level schematic of the SiC AST and (Right, b) Photograph of a fully assembled AST module populated with the SiC Thyristor, Si MOSFETs and the series resistors.

On-state characteristics of the SiC AST

It can be observed from Figure 2(a) that at 100 A/cm^2 and 25 °C, the integrated AST shows a slightly higher Von= 4.0 V as compared to the SiC Thyristor, which has a low Von= 3.8 V. This is due to the additional on-resistance of the series p-MOSFET . From the 25 °C output characteristics at 100 A/cm^2, a higher differential on-resistance of 5.6 mΩ-cm^2 is extracted for the AST in comparison with 3.9 mΩ-cm^2 for the SiC Thyristor. The SiC Thyristor shows a negative temperature co-efficient of Von in Figure 2(a), due to an increase in recombination carrier lifetime and a reduction of the p-n junction knee with temperature. However, the SiC AST shows a slight positive temperature co-efficient of Von because the increase in the on-resistance of the series-connected p-MOSFET opposes the reduction of the knee-voltage of the SiC Thyristor. The current saturation capability of the SiC AST in contrast to the SiC Thyristor is shown through high-current static I-V characteristics in Figure 2(b). At Cathode currents > 90 A (1300 A/cm^2 for the SiC Thyristor), the presence of the Si MOSFET allows for a self- saturation of the AST I-V characteristic, which is a desirable feature for over-current fault protection.

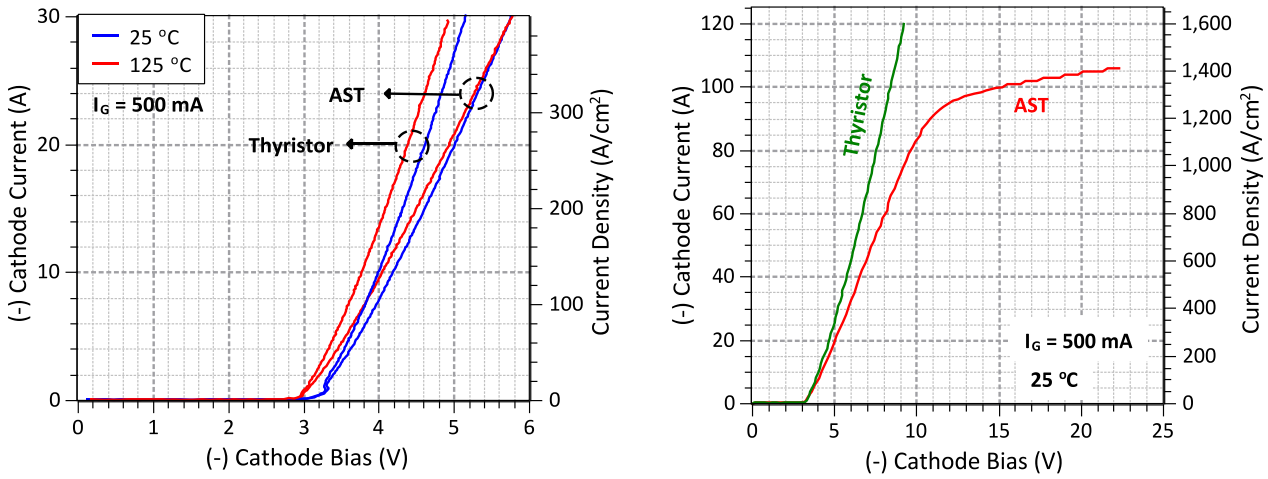

Figure 2: (Left, a) Output characteristics of the SiC AST module and the constituent SiC Thyristor and (Right, b) Current Saturation displayed by the SiC AST at high Cathode current densities.

Blocking characteristics

The open-Gate blocking voltage of the SiC AST was measured to be in excess of 3 kV at 125 °C, limited by the currently used packaging techniques. The blocking characteristics of a 5.25 mm x 5.25 mm, 6.5 kV SiC Thyristor is compared at 25 °C and at 150 °C with a commercial 4 kV Silicon Thyristor in Figure 3. The Si Thyristor displays unacceptably high leakage currents at 125 °C, while only a modest increase in leakage current is measured on the SiC Thyristor at 150 °C, validating the high-temperature operation capability of high-voltage SiC Thyristors.

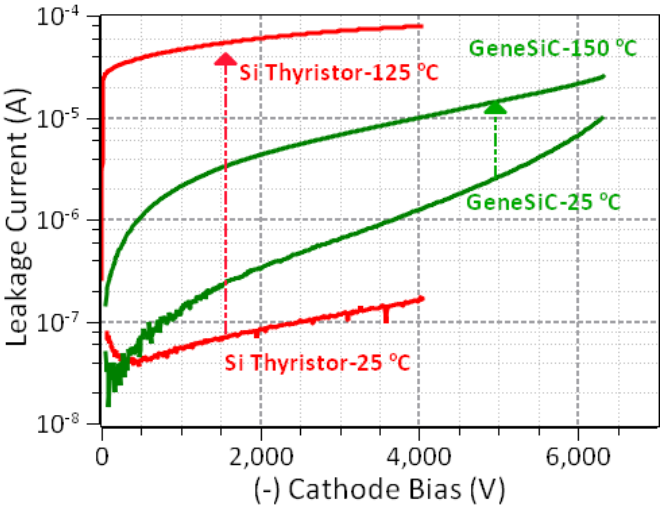

Figure 3: Comparison of blocking characteristics of a 6.5 kV/5.25 mm x 5.25 mm SiC Thyristor with an off-the-shelf 4 kV SiC Thyristor at different temperatures.

AST Switching Characteristics

Detailed AST turn-off voltage and current waveforms are shown in Figure 4(a) and (b) for resistive switching at 1380 V and 20 A. The Gate terminal of the AST was driven between -11 V and 0 V. Referring to Figure 1(a), R_{Anode} = 1 Ω was used for fast turn-on of the Anode p-MOSFET, while R_{Gate} = 10 Ω was used for providing a Gate trigger current of 800 mA to the SiC Thyristor. A small 1 µF charging capacitor was used for applying the Cathode bias to the AST.

Initially, the AST is the blocking state, with most of the 1380 V bias supported across its Anode and Cathode terminals. A very small portion of the applied voltage is supported across the p-MOSFET, which is sufficient to maintain the diode-connected n-MOSFET in the on-state. For turning ON the AST, a (constant) Gate pulse of - 11 V is supplied via an optically isolated Gate driver, which turns on the p-MOSFET, and also establishes a Gate current of ≈ 800 mA for turning ON the SiC Thyristor. Once the sum of voltage drops across the Anode-Gate junction and the p-MOSFET falls below ≈ 4 V, the clamped diode turns-off, and the AST is now in the on-state. A turn-on delay time of 250 ns, a Cathode current rise time of 490 ns and a turn-on dI/dt of 37 A/µs can be noted from Figure 4(a).

For turning OFF the AST, the – 11 V Gate pulse is withdrawn. This results in the p-MOSFET turning off, which results in an increasing voltage drop across the Drain/Source terminals of the p-MOSFET, and consequently the Drain/Source terminals of the diode-connected n-MOSFET. When the + 4 V threshold voltage is exceeded, the n-MOSFET turns ON, the hole injection from the p+ Anode stops, and the entire Thyristor current is commutated through the Gate electrode of the SiC Thyristor (unity-gain turn-off) and the n-MOSFET to ground. The AST turns OFF like an open-base npn transistor, and no Thyristor action is present. This avoids the current filamentation and latch-up problems inherent to standard GTO Thyristors. A Cathode Current fall time of 440 ns and a turn-off dI/dt of 65 A/µs are noted from Figure 4(b). The slow build-up of the

Cathode Bias during device turn-off is due to the small 1 µF charging capacitor used for the measurement. Another useful feature of the AST that can be inferred from Figure 4 is that the Gate terminal of the AST is isolated from the high Cathode currents which are diverted via the Gate electrode of the Thyristor and the series n-MOSFET to ground.

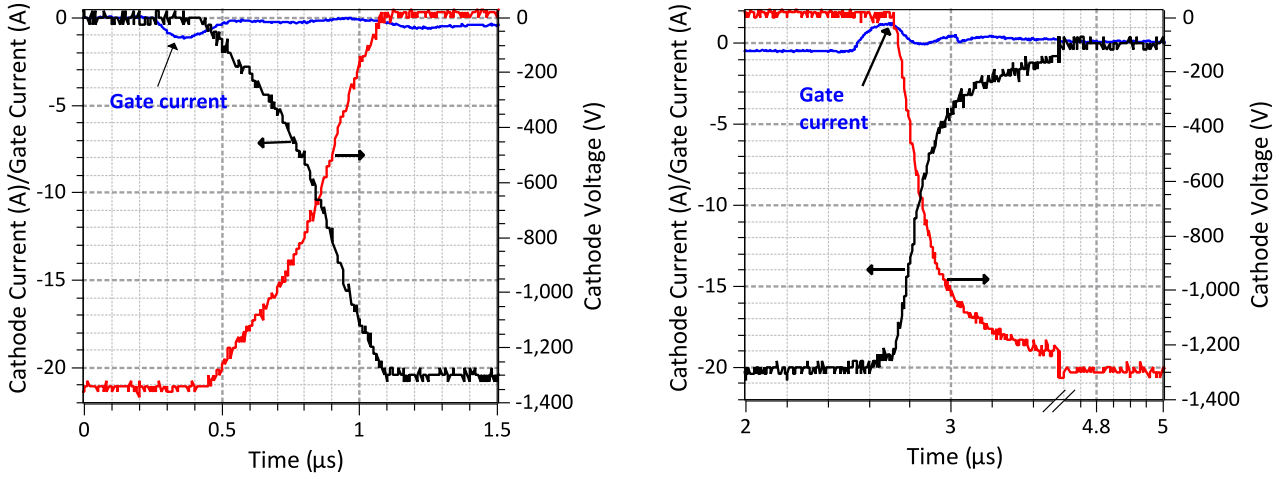

Figure 4 : Current and voltage waveforms obtained (Left a, Turn-ON; and Right b, Turn-OFF) for switching 1.3 kV and 20 A (275 A/cm^2) through the Integrated AST Module.

Ultimate limits of the SiC ASTs

Although this work has only reported on 1380 V and 20 A (275 A/cm^2 for the SiC Thyristor) switching through the SiC AST, switching at much higher current densities is possible for the SiC AST, since the SiC Thyristors do not suffer from dynamic avalanche breakdown mechanism [1] which limits the reverse biased safe operating area (RBSOA) of Si bipolar devices. Dynamic avalanche breakdown occurs, when the injected minority carriers pass through the depleted lower base layer during device turn-off at saturated drift velocity (v_{sat}), thereby increasing the effective base doping concentration, which can be expressed as:

$$N_{eff} \approx N_{A/D} + \frac{J_{load}}{q v_{sat}} \qquad (1)$$

where $N_{A/D}$ is the p-base or n-base (in case of Si Thyristors) doping concentration and J_{load} is the AST load current. This increased base doping concentration increases the slope of the electric field profile and the peak electric field at the p-base/n-base junction, which can reduce the breakdown voltage (BV) from its static avalanche rating. Typical lower base layer N_D values for pnpn Si Thyristors are in the range of 10^{13} cm^{-3}, while a N_A of $5\text{x}10^{14}$ cm^{-3} was used for the npnp SiC Thyristor of this work. Since the v_{sat} values are roughly similar for Si and 4H-SiC ($\approx 1\text{x}10^7$ cm/s), the second term in (1) at a J_{load} of 250 A/cm^2 is calculated as $1.56 \text{ x } 10^{14}$ cm^{-3}, which is ≈ 100 times the N_D in the Si Thyristor but only 0.3 times the N_A of the SiC Thyristor of this work. Thus the dynamic avalanche mechanism severely limits the RBSOA in Si Thyristors, whereas it is not a strong factor in case of 4H-SiC Thyristors.

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References

[1] B. You, A.Q. Huang, Solid-State Electronics, 42(5), 785-794 (1998).